CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:

at least one circuit path sensitive to floating body effects;

a body effect monitor monitoring circuit activity for said at least one circuit path and, selectively providing an indication of said body effect charging responsive to monitored circuit inactivity;

a pulse generator generating a neutralization pulse responsive to an indication of said floating body effects; and

a neutralization pulse distribution circuit selectively providing said neutralization pulse to blocks in said circuit path.

2. An IC as in claim 1, wherein said circuit path is a logic signal path and said blocks are logic blocks.

3. An IC as in claim 2, wherein said neutralization pulse distribution circuit is a shift register comprising a plurality of shift register latches.

4. An IC as in claim 3, wherein said neutralization pulse is sequentially shifted through said plurality of shift register latches.

5. An IC as in claim 3, said IC further comprising:

a test circuit, selectively providing test data for testing said blocks; and

a multiplexor selectively passing data from said test circuit and neutralization pulses from said pulse generator to said shift register.

6. An IC as in claim 1, wherein said circuit path is a random access memory and said blocks are memory cells in a memory array.

7. An IC as in claim 6, wherein said neutralization pulse distribution circuit is a column decode, selecting columns for discharge.

8. An IC as in claim 7, said IC further comprising:

a column select selecting bit lines in said array; and

a column discharge circuit, discharging bit lines selected by said column select.

9. An IC as in claim 8, wherein said body effect monitor provides a neutralization control signal to said column discharge circuit, said column discharge circuit discharging selected said bit lines responsive to said neutralization control signal.

10. An integrated circuit (IC) comprising:

at least one circuit path sensitive to floating body effects, said circuit path including a plurality of logic blocks;

a body effect monitor, monitoring circuit activity for said at least one circuit path and, selectively providing an indication of said floating body effects responsive to monitored circuit inactivity;

a pulse generator generating a neutralization pulse responsive to said indication of body effect charging;

a test circuit, selectively providing test data for testing said logic blocks;

a multiplexor selectively passing data from said test circuit and neutralization pulses from said pulse generator; and

a neutralization pulse distribution circuit receiving selected said test data and said neutralization pulses and passing received said test data and said neutralization pulses to said logic blocks in said circuit path.

11. An IC as in claim 10, wherein said neutralization pulse distribution circuit is a shift register comprising a plurality of shift register latches.

12. An IC as in claim 11, wherein said neutralization pulse is sequentially shifted through said plurality of shift register latches.

13. An IC as in claim 12, wherein said shift register is a test register.

14. A random access memory (RAM) comprising:

a memory array comprising a plurality of memory cells organized as a plurality of rows and columns;

a word decoder selecting a word line identifying one of said rows responsive to a memory location access request;

a column decoder providing a column select signal responsive to said memory location access request;

a column select selecting a column responsive to said column select signal;

a pulse generator generating a neutralization pulse responsive to an indication of said floating body effects;

a neutralization pulse distribution circuit selectively providing said neutralization pulse to said column decoder as said memory location access request; and

a column select discharge discharging bit lines in a corresponding array column selected by said column select.

15. A RAM as in claim 14, wherein each of said columns includes a plurality of said bit lines.

16. A RAM as in claim 15, wherein said column select is a plurality of pass gate pairs, each of said pass gate pairs connected to one of said plurality of bit lines.

17. A RAM as in claim 15, wherein said column select discharge is a plurality of field effect transistor (FET) pairs, each of said FET pairs connected to a plurality of said pass gate pairs.

18. A RAM as in claim 17, wherein said plurality of memory cells are static RAM (SRAM) cells.

19. A method of maintaining performance in an integrated circuit (IC), said method comprising:

a) monitoring circuit activity for said at least one circuit path and selectively providing an indication of said floating body effects;

b) generating a neutralization pulse responsive to an indication of said floating body effects;

c) selectively providing said neutralization pulse to blocks in said circuit path; and

d) neutralizing said floating body effects in each selected said block.

20. A method as in claim 19, wherein circuit activity is being monitored for said floating body effects in a logic path and the step (c) of selectively providing said neutralization pulse comprises selecting between test data from a test circuit and said neutralization pulse.

21. A method as in claim 20, wherein the step (c) of selectively providing said neutralization pulse further comprises receiving said neutralization pulse from a prior block neutralization circuit and passing said neutralization pulse to a subsequent block neutralization circuit.

22. A method as in claim 19, wherein circuit activity being monitored for said floating body effects is memory access and the step (c) of selectively providing said

neutralization pulse comprises selecting a cell column while holding all memory word lines unselected.

23. A method as in claim 22, wherein the step (c) of selectively providing said neutralization pulse further comprises sequentially selecting each said cell column.

24. A method as in claim 23, wherein the step (c) of selectively providing said neutralization pulse further comprises grounding column lines for each selected said cell column.

25. A method as in claim 22, wherein the step (a) of monitoring circuit activity begins after a memory location access.

26. A method as in claim 25, wherein the step (a) of monitoring circuit activity restarts after each said memory location access.